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EXAMINER

WHIPKEY, JASON T

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/648,403

Applicant(s)

TSAI, RICHARD H.

Examiner

Jason T. Whipkey

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 October 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-30 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 24 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Change of Examiner***

1. The examiner of record for this application has been changed to Jason Whipkey. Any inquiry regarding this application should be directed to the new examiner. Current contact information is provided in the last section of this communication.

### ***Response to Arguments***

2. Applicant's arguments — see the third paragraph on page 2 — filed October 12, 2004, with respect to the rejection of claims 1-30 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Chen.

### ***Claim Objections***

3. Claim 17 is objected to as failing to comply with 37 CFR 1.75(a) for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites the limitation "said pair of p+ type guard rings" on lines 3-4. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the claim will be treated as if it is dependent on claim 16.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6, 10, 14, 15, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (U.S. Patent No. 5,869,857).

Regarding **claim 1**, Chen discloses a pixel sensor (see Figure 17A) comprising:

an n-type photosensitive element (the photodiode shown in Figure 17A is an n+ node formed in a p-type substrate; see column 11, line 67, through column 12, line 2) for converting an optical image to an electrical signal;

a p-type source follower transistor (M1 in Figure 17A; see also column 4, line 54) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a readout circuit coupled to said source follower transistor and comprising a p-type transistor (M2 in Figure 17A; see also column 12, line 4); and

a first reset circuit configured to provide a reset signal at said gate of said source follower transistor, where said first reset circuit includes at least one p-type transistor (M3 in Figure 17A; see also column 11, lines 27-28).

Regarding **claim 2**, Chen discloses:

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said p-type transistors are MOSFET p-type transistors (see the symbol in Figure 17A and column 12, line 1).

Regarding **claim 3**, Chen discloses:

said n-type photosensitive element is an n-type photodiode (see the symbol in Figure 17A and column 11, line 67).

Regarding **claim 6**, Chen discloses:

a p-type substrate in which said n-type photosensitive element is formed (see column 11, line 67, through column 12, line 1).

Regarding **claim 10**, Chen discloses an image sensing device (see Figure 17A), comprising:

a p-type substrate (see column 11, line 67, through column 12, line 1);  
an n-type photodiode formed in said p-type substrate (the photodiode shown in Figure 17A is an n<sup>+</sup> node formed in a p-type substrate; see column 11, line 67, through column 12, line 2) where said n-type photodiode operates to convert an optical image to an electrical signal;

a p-type source follower transistor (M1 in Figure 17A; see also column 4, line 54) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a first reset circuit configured to provide a reset signal for said electrical signal, said first reset circuit including a p-type MOSFET transistor (M3 in Figure 17A; see also column 11, lines 27-28); and

a readout circuit operating to buffer said electrical signal (see Figure 17A, which has the buffer circuitry fully described in column 10, lines 27-34, with regard to Figure 12A), said readout circuit including a p-type MOSFET transistor (M4 in Figure 17A).

Regarding **claim 14**, Chen discloses a CMOS image sensor system, comprising:

an array of active pixel sensors (each pixel is fabricated in CMOS and has an amplifier; see column 12, lines 1-2), each pixel sensor of said array including:

an n-type photosensitive element (the photodiode shown in Figure 17A is an n+ node formed in a p-type substrate; see column 11, line 67, through column 12, line 2) operating to convert an optical image to an electrical signal;

a p-type source follower transistor (M1 in Figure 17A; see also column 4, line 54) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

a pixel readout circuit (see Figure 17A, which has the buffer circuitry fully described in column 10, lines 27-34, with regard to Figure 12A), where said pixel readout circuit includes at least one p-type transistor coupled to receive an output of said source follower transistor; and

a first reset circuit configured to provide a reset level for a pixel output signal, where said first reset circuit includes at least one p-type transistor (M3 in Figure 17A; see also column 11, lines 27-28);

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a control circuit configured to provide timing and control signals to enable read out of data stored in said array of active pixel sensors (in order for the pixel shown in Figure 17A to be operable, it is inherent that some sort of control circuitry is present); and

a column readout circuit operating to receive and process said data stored in said array of active pixel sensors (it is inherent that in order for the pixel shown in Figure 17A to be operable, it is inherent that some sort of column readout circuitry is inherent to receive and assemble the data into a useful form).

Regarding **claim 15**, Chen discloses:

a p-type substrate in which said array of pixel sensors is formed (see column 11, line 67, through column 12, line 1).

Regarding **claim 22**, Chen discloses:

said source follower transistor is a p-type MOSFET transistor (M1 in Figure 17A; see also column 4, line 54).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Chou (U.S. Patent No. 6,252,218).

**Claims 4 and 5** may be treated like claim 3. However, Chen is silent with regard to forming the n-type photodiode in a square or circular layout design.

Chou discloses an active pixel image sensor in which photodiodes are laid out in a geometrically-efficient pattern (see figures 6, 7, 9, and 11 and column 4, lines 9-43). As stated in column 4, lines 14-17, an advantage to using such layouts is that noise and crosstalk may be reduced. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include pixels laid out in a square or circular layout design, such as in the way described by Chou.

8. Claims 7, 11, 16, 21, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Akagawa (U.S. Patent No. 5,757,008).

**Claims 7, 11, and 16** may be treated like claims 6, 10, and 15, respectively. However, Chen is silent with regard to forming a pair of p+ type guard rings in the p-type substrate.

Akagawa discloses a pixel sensor, including:

a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photosensitive element (see figures 7 and 9-11).

An advantage to including a guard ring is that a guard ring prevents interference from adjacent components. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include the guard rings described by Akagawa.

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Akagawa is silent with regard to with regard to connecting the guard rings to a ground voltage.

Official Notice is taken that guard rings are commonly grounded. An advantage to doing so is that leakage current can be further reduced. For this reason, it would have been obvious at the time of invention to ground Akagawa's guard rings.

**Claims 21 and 27** may be treated like claims 10 and 14, respectively. Additionally, Chen teaches that each pixel is fabricated in CMOS (see column 12, lines 1-2). However, Chen is silent with regard to the p-type transistors providing radiation hardness without any radiation protective enclosure.

Akagawa discloses a CMOS image sensing device, wherein p-type transistors provide radiation hardness without any radiation protective enclosure (see column 21, line 65, through column 22, line 62). An advantage to providing such protection without an enclosure is that fewer components are necessary in manufacture. For this reason, it would have been obvious at the time of invention to have Chen's image sensor provide radiation hardness without any radiation-protective enclosure.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Merrill (U.S. Patent No. 6,369,853).

**Claim 8** may be treated like claim 6. However, Chen is silent with regard to connecting the n-type well to a supply voltage.

Merrill discloses an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent charges from escaping the pixel sensor (see column 7, lines 28-47, and column 8, lines 23-44).

As stated in column 8, lines 39-42, an advantage to connecting a supply voltage is that the loss of charge is prevented. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include an n-type well connected to a supply voltage, such as the one described by Merrill.

10. Claims 9, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Merrill (U.S. Patent No. 5,917,547).

**Claims 9, 13, and 18** may be treated like claims 1, 10, and 14, respectively. However, Chen is silent with regard to including a second reset circuit.

Merrill discloses an active pixel sensor in Figure 2, wherein:

a second reset circuit having a p-type MOSFET transistor (PMOS transistor P3 in Figure 2; see column 6, lines 21-30) coupled to an input of said first reset circuit, said second reset circuit allowing pixel-by-pixel reset operation (a pixel can inherently be reset only when Reset1 and Reset2 are both in appropriate states).

As stated in column 6, lines 28-30, an advantage to including a second reset transistor is that variation in the voltage of the photodiode/reset transistor node can be reduced. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include a second reset circuit, such as the one described by Merrill.

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11. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Akagawa and further in view of Merrill '853.

**Claims 12 and 17** may be treated like claims 11 and 16, respectively. However, Chen is silent with regard to connecting the n-type well to a supply voltage.

Merrill discloses an n-type well formed in said p-type substrate, said n-type well adapted for connection to a supply voltage, and operating to prevent crosstalk between pixels in the image sensing device (see column 7, lines 28-47, and column 8, lines 23-44).

As stated in column 8, lines 39-42, an advantage to connecting a supply voltage is that the loss of charge is prevented. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include an n-type well connected to a supply voltage, such as the one described by Merrill.

12. Claims 19, 20, 23, 24, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen.

**Claims 19, 23, and 25** may be treated like claims 1, 19, 10, 23, 14, and 25, respectively. However, Chen is silent in the embodiment shown in Figure 17A with regard to readout switch M2 being controlled by row.

In a similar embodiment shown in Figure 11A, Chen shows readout switches M2 connected to vertical shift register Y row by row.

An advantage to connecting rows of readout switches together is that the control circuitry (in this case, vertical shift register Y) need not control readout pixel by pixel, thus reducing

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system complexity. For this reason, it would have been obvious at the time of invention to have the embodiment disclosed by Chen in Figure 17A include readout controlled by rows.

Regarding **claims 20, 24, and 26**, Chen shows in Figure 17A that readout switch M2 (see column 12, line 4) is connected to the output of source follower M1.

13. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Merrill '547 and further in view of Akagawa.

Regarding **claim 28**, Chen discloses a pixel sensor comprising:

- a plurality of pixels formed in a p-type substrate (see column 11, line 67, through column 12, line 2), at least one of said pixels comprising:

- an n-type photodiode formed in said substrate (the photodiode shown in Figure 17A is an n<sup>+</sup> node formed in a p-type substrate; see column 11, line 67, through column 12, line 2) and for generating an electrical signal in response to an applied optical image;

- a p-type source follower transistor (M1 in Figure 17A; see also column 4, line 54) for receiving said electrical signal at a gate thereof and for producing therefrom a pixel output signal;

- a first reset circuit coupled to said gate and responsive to a first reset signal for providing a global reset value as said pixel output signal (M3 in Figure 17A; see also column 11, lines 27-28);

- a p-type row select transistor (M2 in Figure 17A; see also column 12, line 4);

Chen is silent with regard to including a second reset circuit.

Merrill discloses an active pixel sensor in Figure 2, wherein:

a second reset circuit (PMOS transistor P3 in Figure 2; see column 6, lines 21-30) coupled to an input of said first reset circuit and responsive to a second reset signal for operating said first reset circuit to allow a pixel-by-pixel reset (a pixel can inherently be reset only when Reset1 and Reset2 are both in appropriate states).

As stated in column 6, lines 28-30, an advantage to including a second reset transistor is that variation in the voltage of the photodiode/reset transistor node can be reduced. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include a second reset circuit, such as the one described by Merrill.

Chen is also silent in the embodiment shown in Figure 17A with regard to readout switch M2 being controlled by row.

In a similar embodiment shown in Figure 11A, Chen shows readout switches M2 connected to vertical shift register Y row by row, causing the pixels to output to column lines.

An advantage to connecting rows of readout switches together is that the control circuitry (in this case, vertical shift register Y) need not control readout pixel by pixel, thus reducing system complexity. For this reason, it would have been obvious at the time of invention to have the embodiment disclosed by Chen in Figure 17A include readout controlled by rows.

Chen is silent with regard to forming a pair of p+ type guard rings in the p-type substrate.

Akagawa discloses a pixel sensor, including:

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a pair of p+ type guard rings formed in said p-type substrate, each of said pair of guard rings formed on either side of said n-type photodiode (see figures 7 and 9-11).

An advantage to including a guard ring is that a guard ring prevents interference from adjacent components. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include the guard rings described by Akagawa.

Regarding **claim 30**, Chen is silent with regard to the p-type transistors providing radiation hardness without any radiation protective enclosure.

Akagawa discloses a CMOS image sensing device, wherein p-type transistors provide radiation hardness without any radiation protective enclosure (see column 21, line 65, through column 22, line 62). An advantage to providing such protection without an enclosure is that fewer components are necessary in manufacture. For this reason, it would have been obvious at the time of invention to have Chen's image sensor provide radiation hardness without any radiation-protective enclosure.

14. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Merrill '547 and further in view of Akagawa and Merrill '853.

**Claim 29** may be treated like claim 28. However, Chen is silent with regard to including an n-type well located adjacent to the guard rings.

Merrill '853 shows in Figure 9B an n-type well 220 located adjacent to guard rings 214 and 218 in a p-type substrate (see column 9, line 44, through column 10, line 45).

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An advantage to including n-type wells is that a loss of pixel charge may be prevented. For this reason, it would have been obvious at the time of invention to have Chen's image sensor include an n-type well, such as the one described by Merrill.

### *Conclusion*

15. Applicant's amendment on April 20, 2004, necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

16. Any inquiry concerning this communication or earlier communications should be directed to Jason Whipkey, whose telephone number is (703) 305-1819. The examiner can

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normally be reached Monday through Friday from 8:30 A.M. to 6:00 P.M. eastern standard time, alternating Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber, can be reached on (703) 305-4929. The fax phone number for the organization where this application is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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December 18, 2004

  
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